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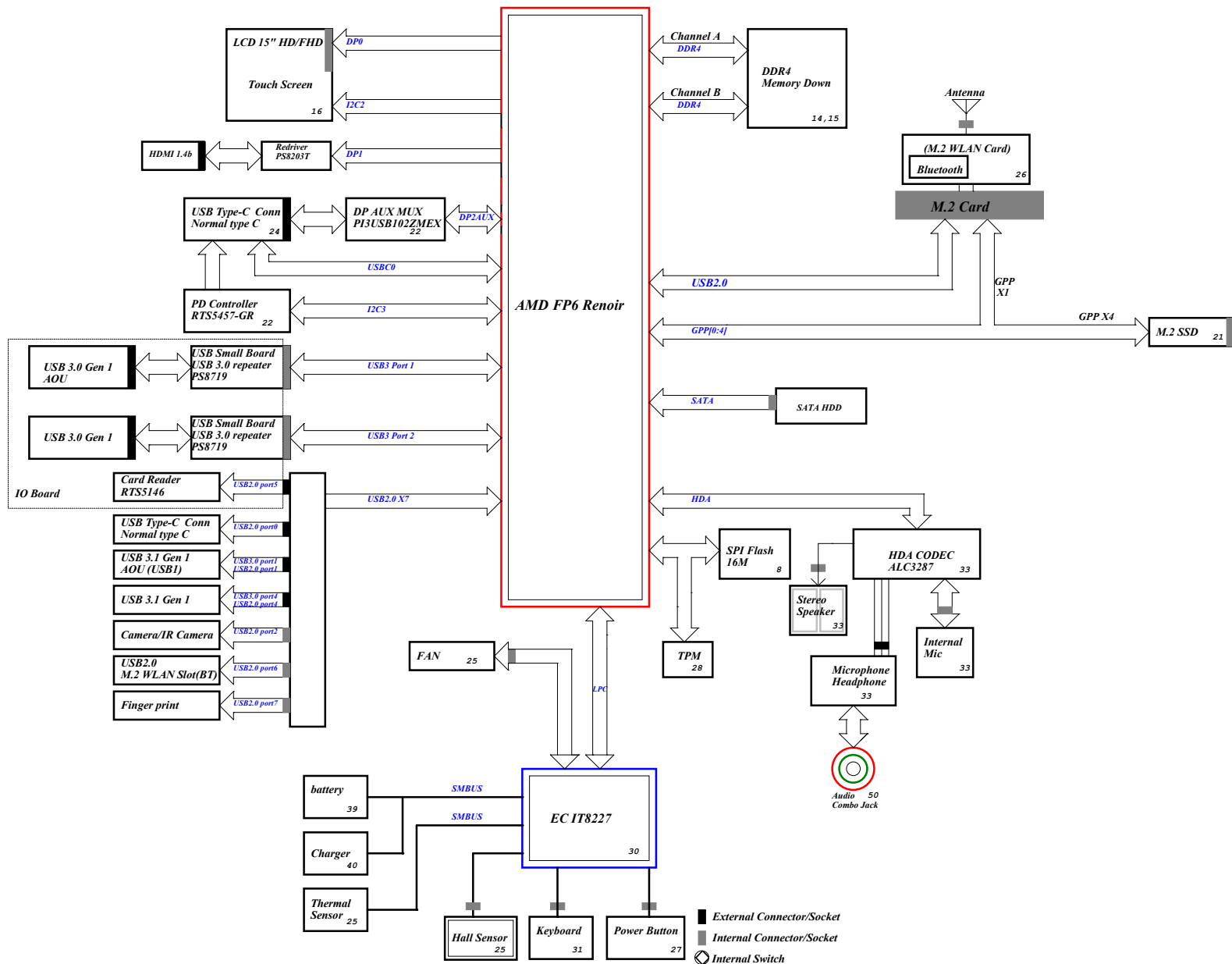
S550 Renoir M/B Schematics Document

AMD FP6 Renoir with DDR4

2019-03-12

REV: 0.1

Security Classification	LC Future Center Secret Data			Title	
Issued Date	2019/02/27	Deciphered Date	2020/02/27	Cover Page	
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<div>power plane</div> <div>State</div>	<div>B+ (+20VSB)</div> <div>+3VL</div> <div>+5VLP</div>	<div>+5VALW</div> <div>+3VALW (+3VALW_APU)</div> <div>+1.8VALW</div> <div>+0.75VALW</div>	<div>+2.5V</div> <div>+1.2V</div>	<div>+5VS</div> <div>+3VS</div> <div>+1.8VS</div> <div>+0.75VS</div> <div>+0.6VS</div> <div>+VDDC_VDD</div> <div>+VDDCR_SOC</div>
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

	SOURCE	PD	BATT	IT8227	EXPAND	WLAN	Thermal Sensor	APU	Charger	PMIC
EC_SMB_CK0 EC_SMB_DA0	IT8227 +3VL	X	X		X	X	V +3VS	V +3VS	X	X
EC_SMB_CK1 EC_SMB_DA1	IT8227 +3VL	X	V +3VL		X	X	X	X	V +3VL	X
EC_SMB_CK2 EC_SMB_DA2	IT8227 +3VS	V +3VL	X		X	X	X	X	X	X
EC_SMB_CK3 EC_SMB_DA3	IT8227 +3VL	X	X		X	X	X	X	X	V +3VL

Device	Address
PD	
PMIC	0X34

Device	Address
Charger	0b00010010
Battery	?

Device	Address
APU SB-TSI	releate to F3x1E4[\$biAddr] or Address Select Pins setting
Thermal Sensor	10011011b(read) 10011010b(write)

Device	Address
Expand IT8013	0100,A2,A1,A0

	<i>SOURCE</i>	<i>Device</i>
<i>TP_I2C2_SCL</i>	<i>APU</i>	<i>Touch Screen</i>
<i>TP_I2C2_SDA</i>	<i>+3VS</i>	<i>+3VS</i>

Device	Address
	?
	?

	SOURCE	DEVICE
TP_I2C3_SCL	APU	Touch Pad
TP_I2C3_SDA	+3VALW	+3VS


Device	Address
Elan: SA469D-22HA 69x104x1.0	?
Synaptics: TM-P3255-008 69x104x1.0	?

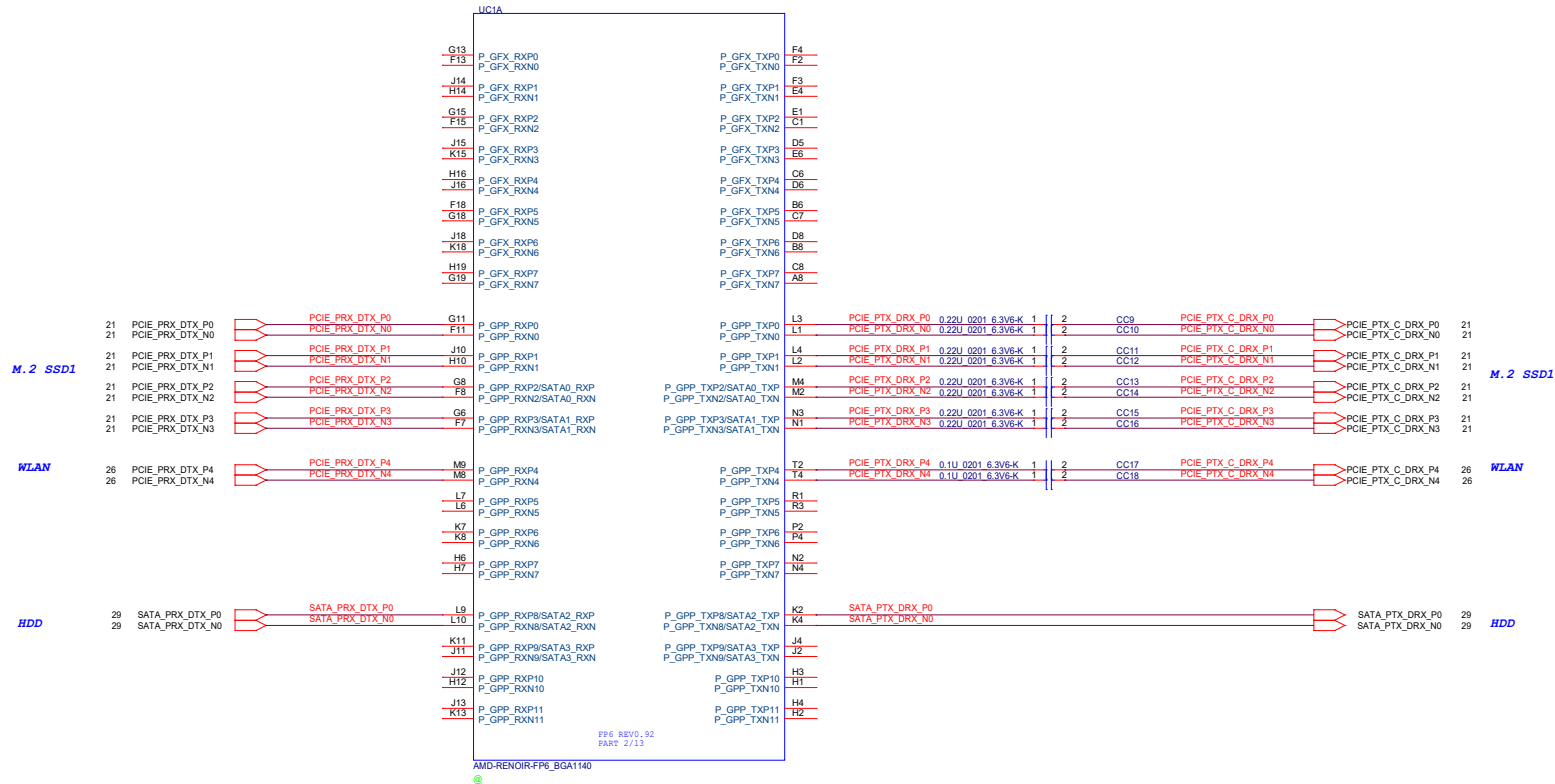
	SOURCE	DEVICE
USBC_I2C_SCL	APU	PD Controller
USBC_I2C_SDA	+1.8VALW	+5VALW

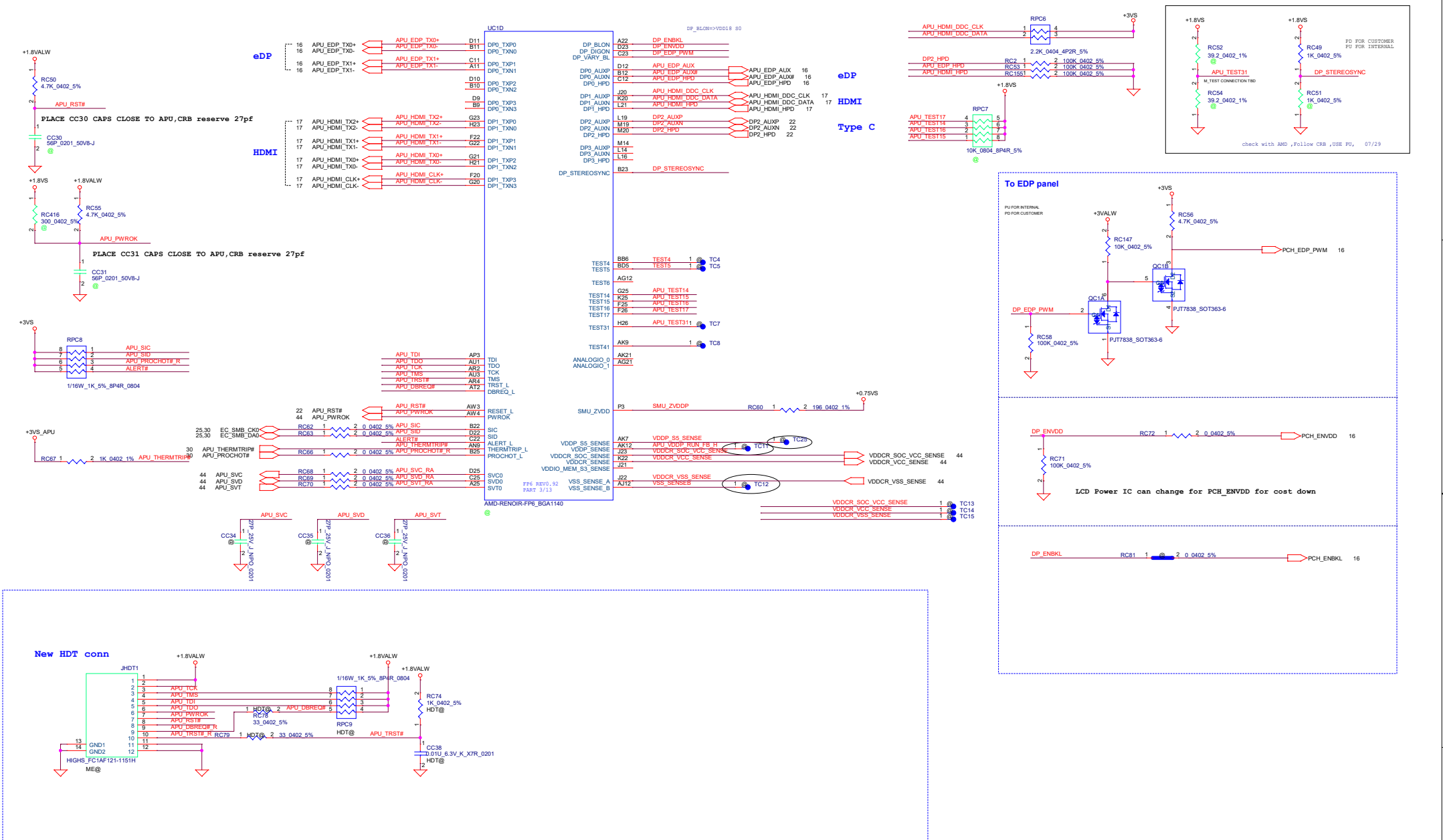
Device	Address
	?

HSIO Port		Device
GFX	0	N/A
	1	
	2	
	3	
	4	
	5	
	6	
GPP	7	<div>SSD</div> <div>WLAN</div> <div>N/A</div> <div>HDD</div> <div>N/A</div>
	0	
	1	
	2	
	3	
	4	
	5	
	6	
	7	
	8	
	9	
USB3.0	10	<div>Type C</div> <div>USB 3.0 (AOU)</div> <div>USB 3.0 (Normal)</div> <div>N/A</div>
	0	
	1	
	4	
	5	
USB2.0	6	<div>Type C</div> <div>USB 3.0 (AOU)</div> <div>Camera</div> <div>Touch Screen</div> <div>USB 3.0 (Normal)</div> <div>Cardreader</div> <div>BT</div> <div>Finger Print</div>
	0	
	1	
	2	
	3	
	4	
	5	
	6	

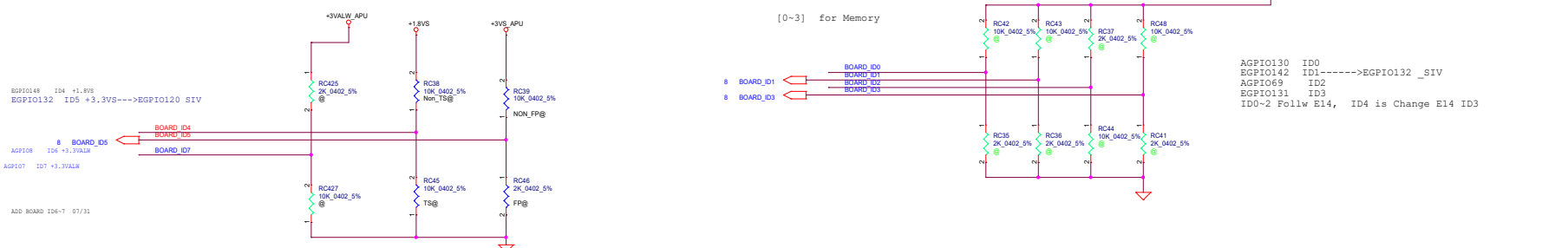
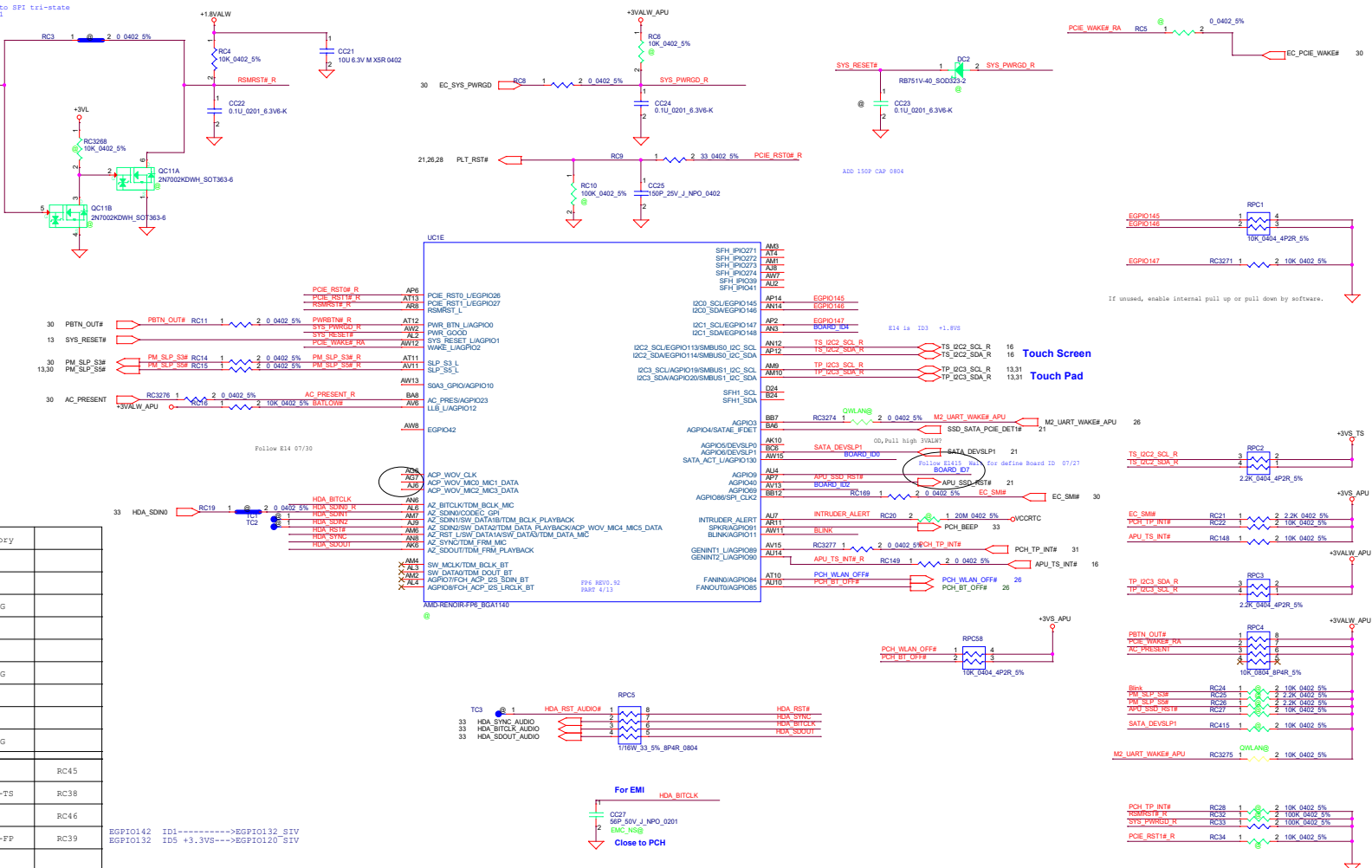
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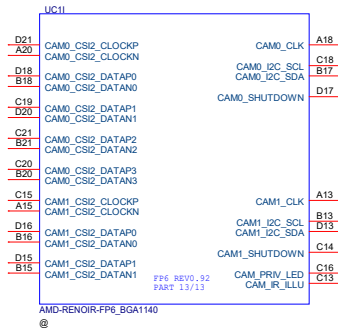
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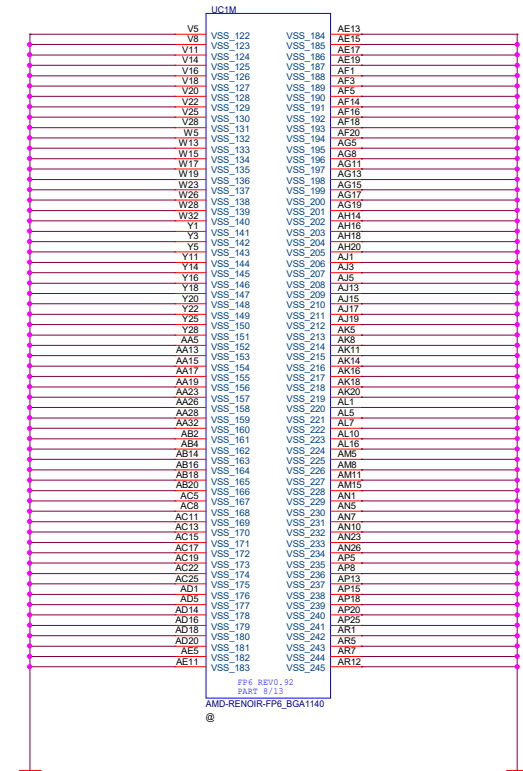
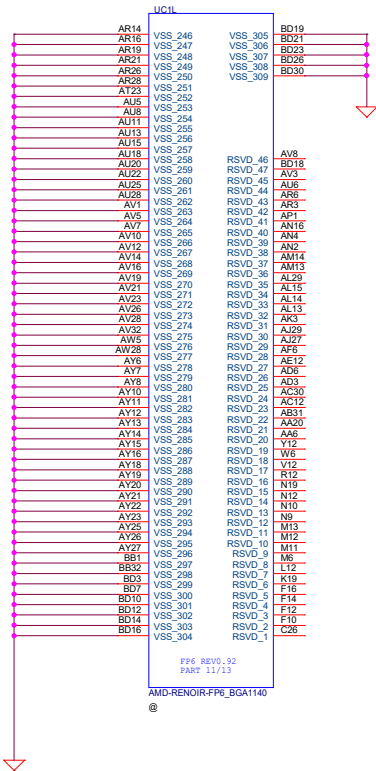
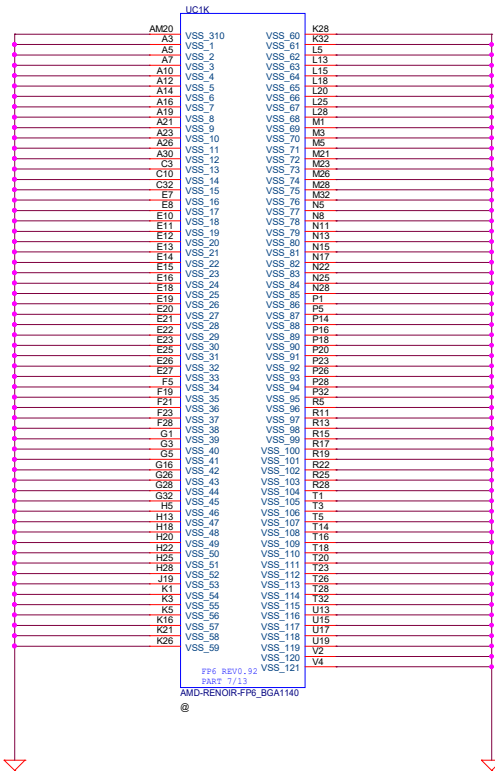


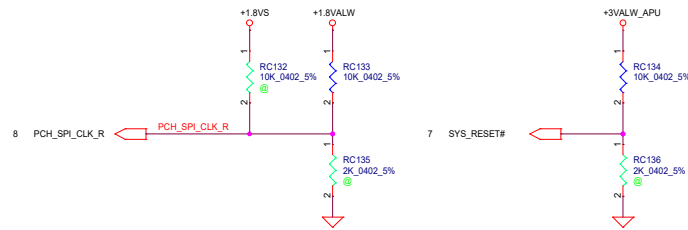


Board ID[0:1]	Board ID[2:3]	Memory	
00 Samsung	00	4G	
	01	8G	
	10	16G	
01 Micron	00	4G	
	01	8G	
	10	16G	
10 Hynix	00	4G	
	01	8G	
	10	16G	
Board_ID4	0	TS	RC45
	1	NON-TS	RC38
Board_ID5	0	FP	RC46
	1	NON-FP	RC39
Board_ID6	Reserved		
	Reserved		
Board_ID7	Reserved		
	Reserved		



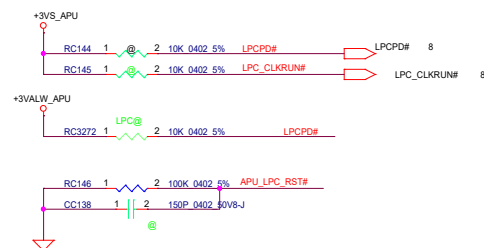
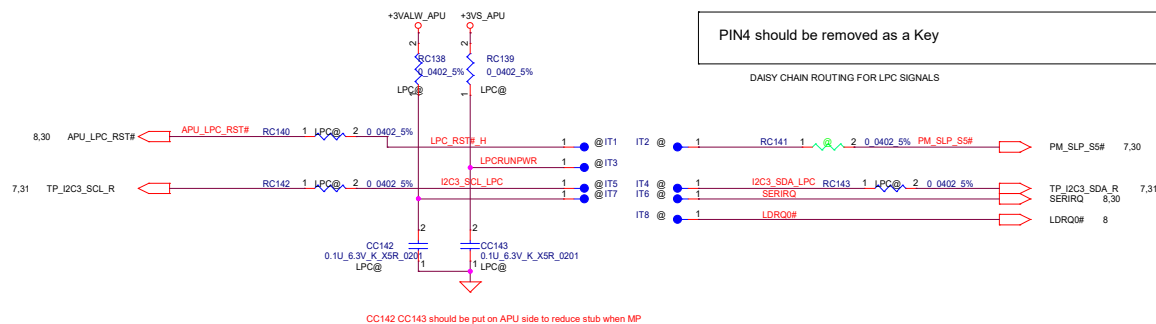




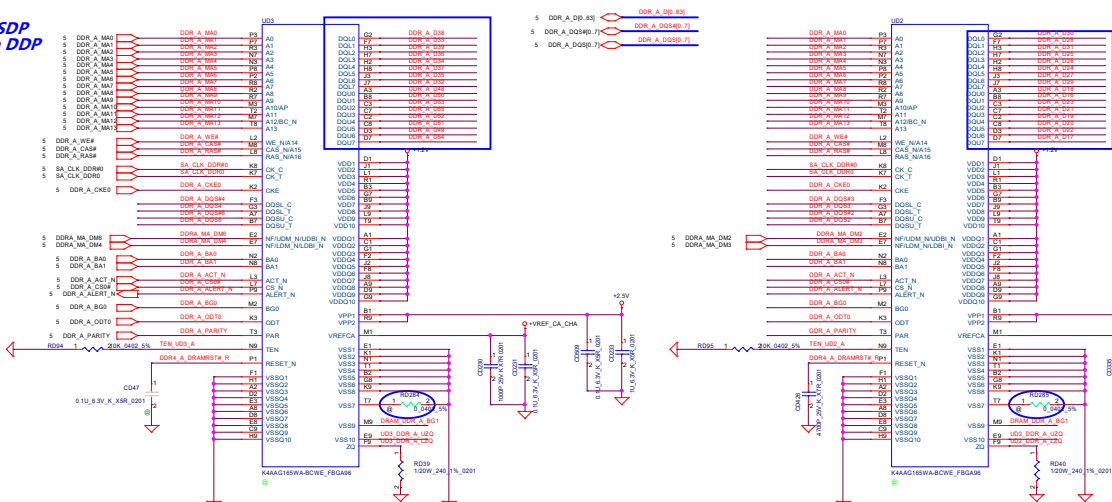


STRAP PINS	SYS_RESET#
PCH_SPI_CLK	1:USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS (DEFAULT) 0:USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RESET#	1:NORMAL RESET MODE (DEFAULT) 0:SHORT RESET MODE

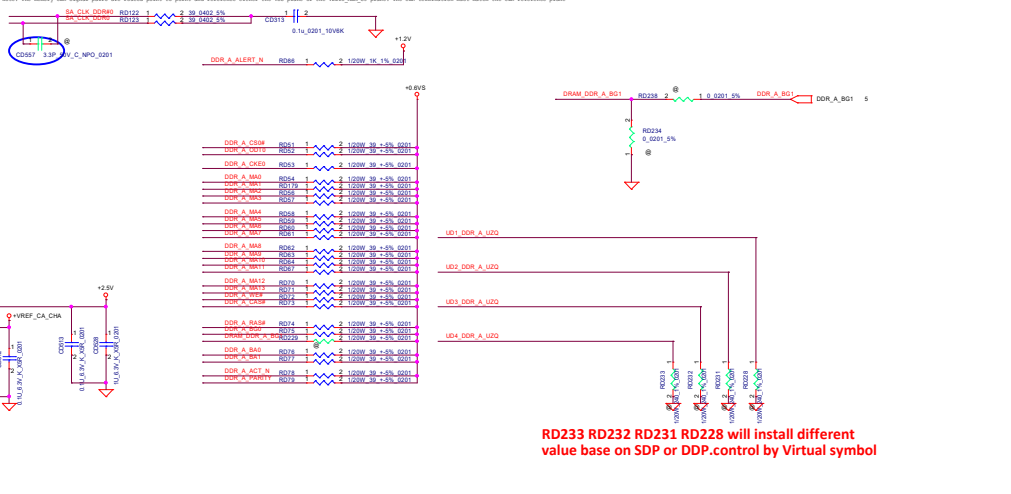
LPC ROM EMULATOR HEADER



8Gb SDP
16Gb DDP



Note: The memory CDF signal pairs are routed point to point and reference within the VSS plane or the VDDIO/MEM_S3 plane. The CDF termination must match the CDF reference plane.



RD233 RD232 RD231 RD228 will install different value base on SDP or DDP, control by Virtual symbol

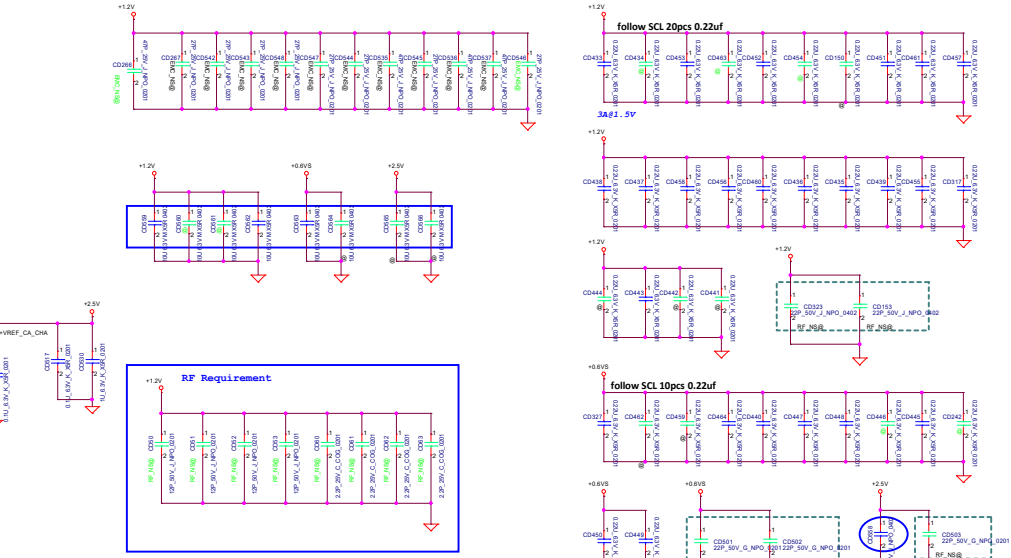
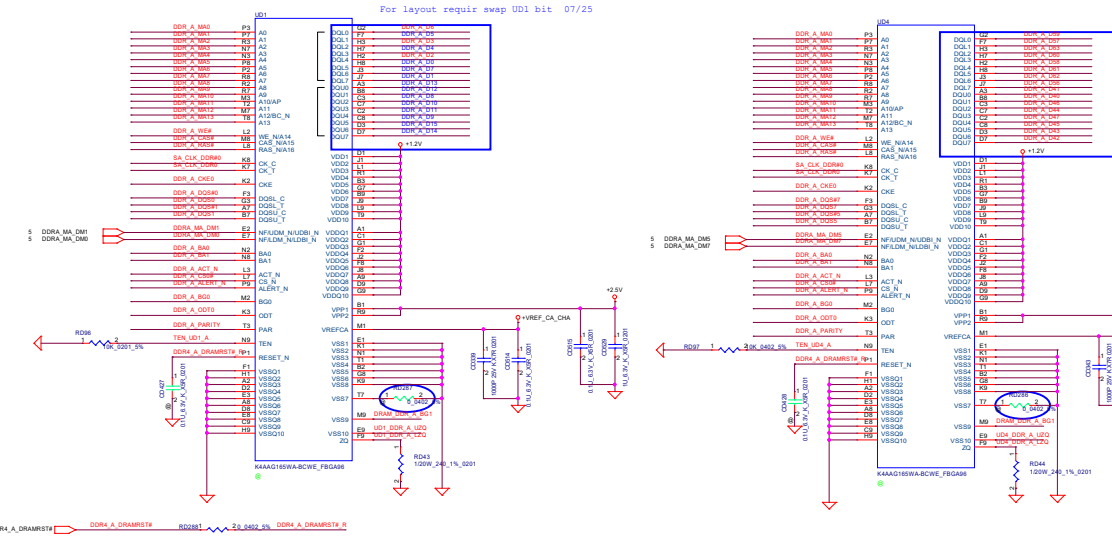


Table 32. DDR4 DRAM Down Per-Channel Decoupling Capacitors

Capacitor	Configuration	VDDIO_MEM_S3-VSS	VDDIO_MEM_S3-VTT	VTT-VSS	VREF_CA-VDDIO_MEM_S3
Value	Package Size / Material				
0.1 µF	0402 XSR	SRx16	-	-	-
0.22 µF	0402 XSR	SRx16	18	5	5

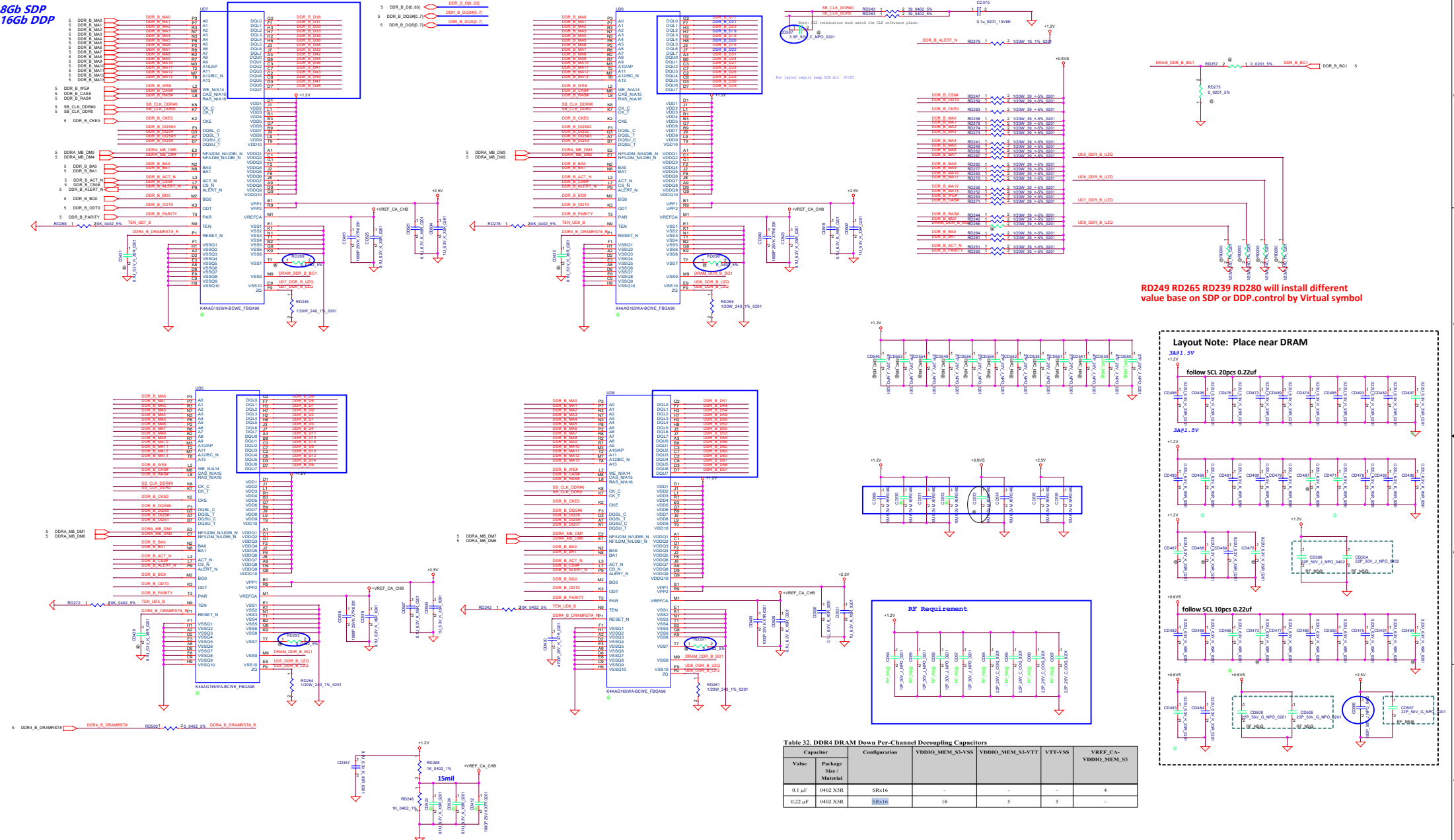
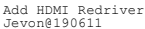




Table 32. DDR4 DRAM Down Per-Channel Decoupling Capacitors

Capacitor	Configuration	VDDIO_MEM_S3-VSS	VDDIO_MEM_S3-VTT	VTT-VSS	VREF_CA_VDDIO_MEM_S3
Value	Package Size / Material				
0.1 μ F	0402 N3R	SRx16	-	-	4
0.22 μ F	0402 N3R	SRx16	18	5	-



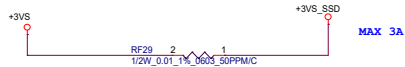
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5		4		3		2		1	
D								D	
C								C	
B								B	
A								A	

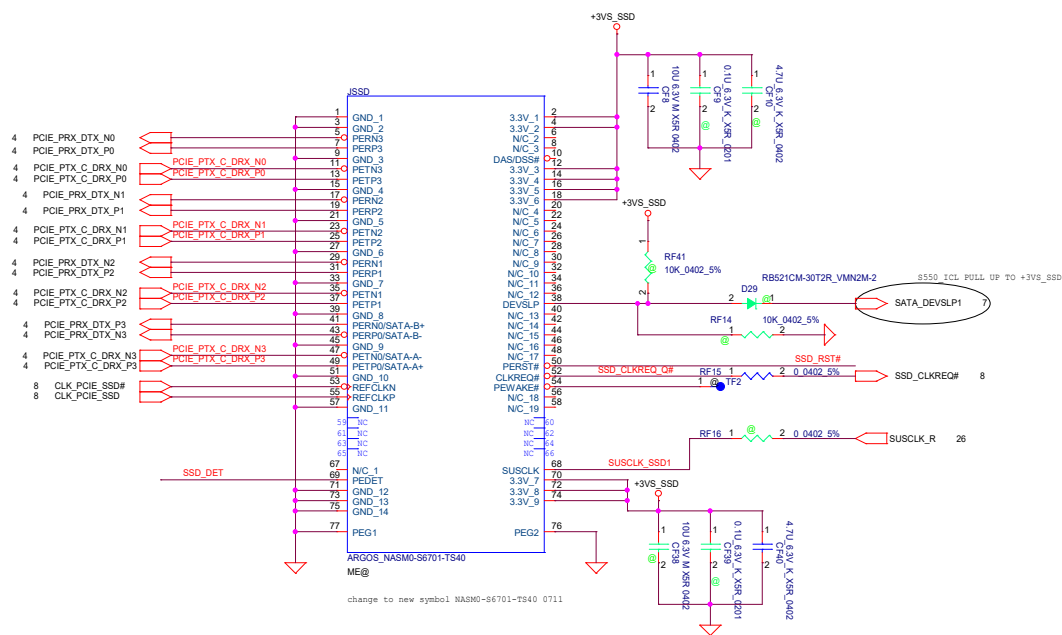
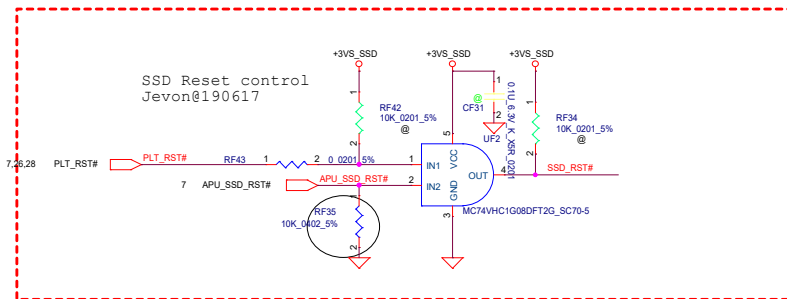
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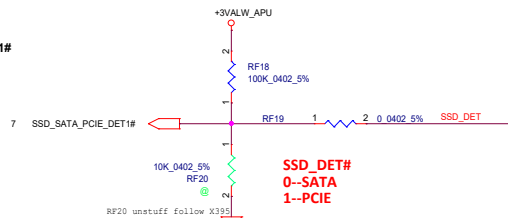


Change RF29 0603 R to J14 07/27
Follow S550 intel use precision resistor 0802



change to new symbol NASMO-86701-TS40 0711

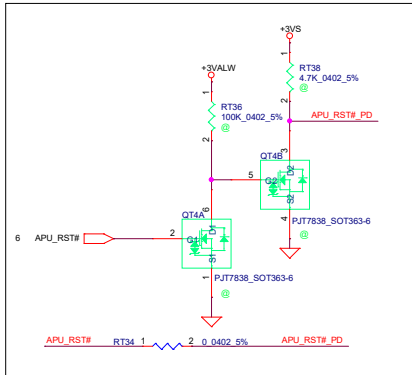
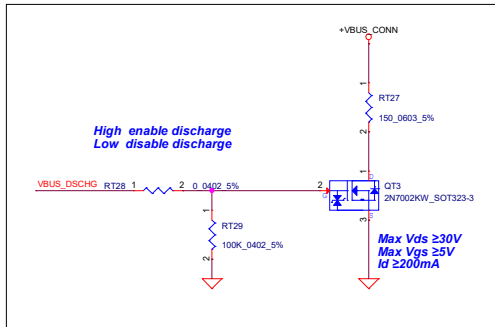
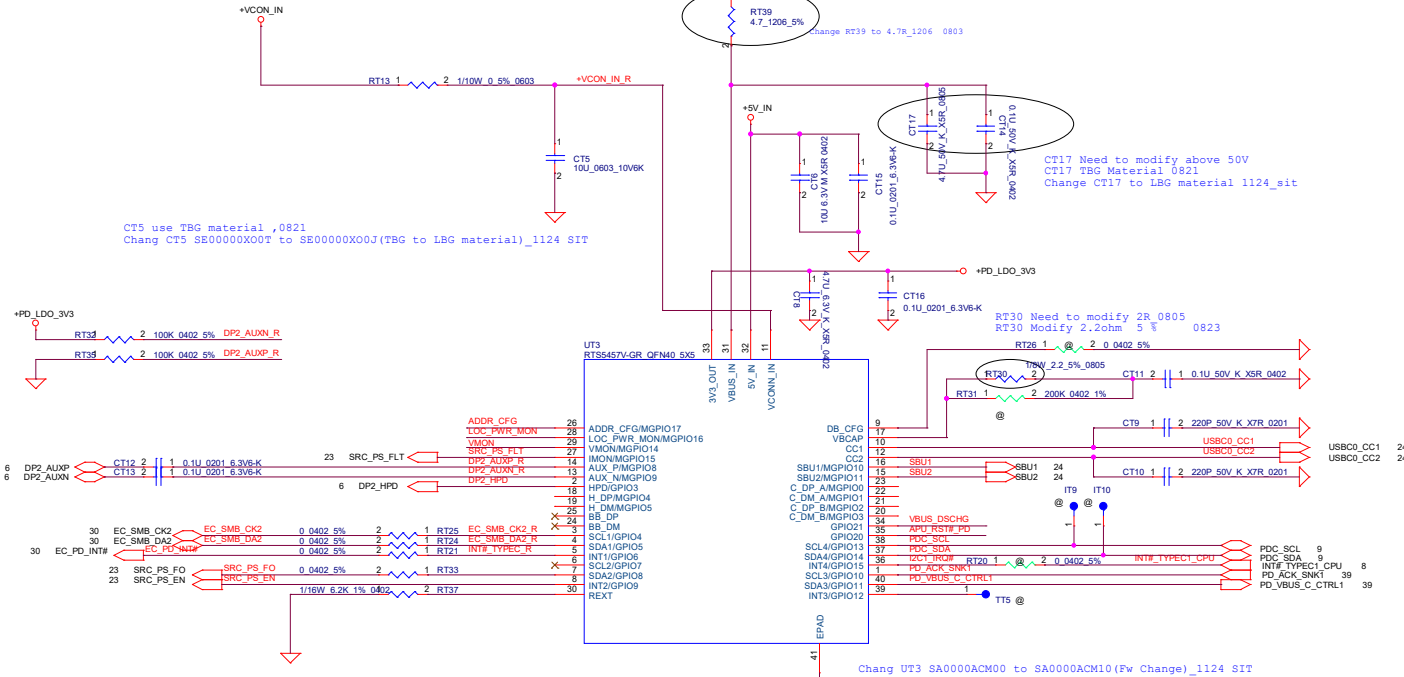
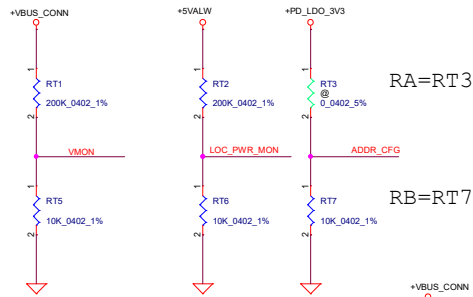
SSD_SATA_PCIE_DET1#
SATA Device GND
PCIe Device NC

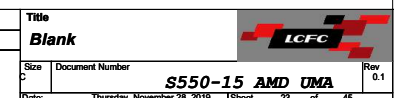
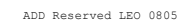


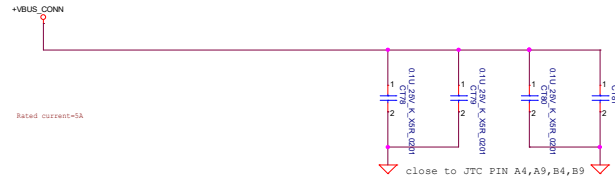
SSD_DET#
0--SATA
1--PCIe

RF20 unstuff follow X395

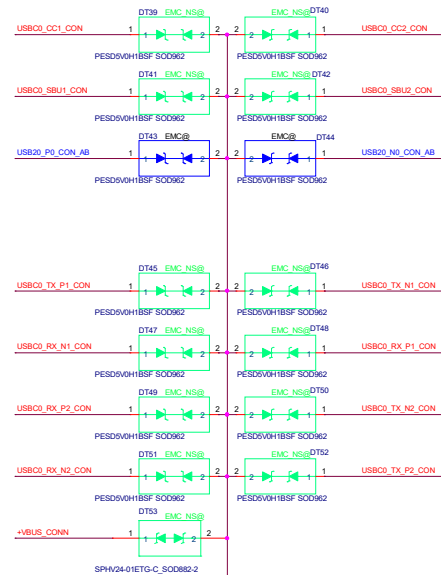
Slave Addr	Ra 1%	Rb 1%
addr0	NC	10K
addr1	54.9K	12.1K
addr2	27.4K	15.8K
addr3	18.2K	22.1K



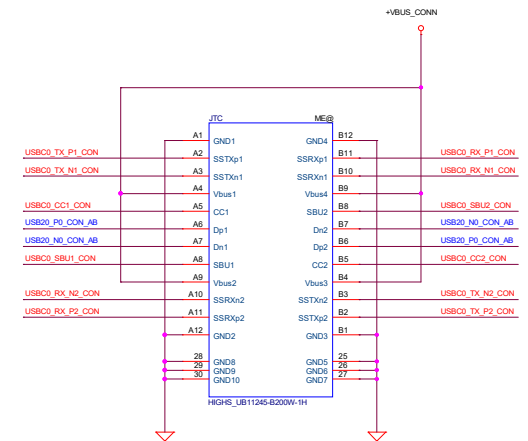






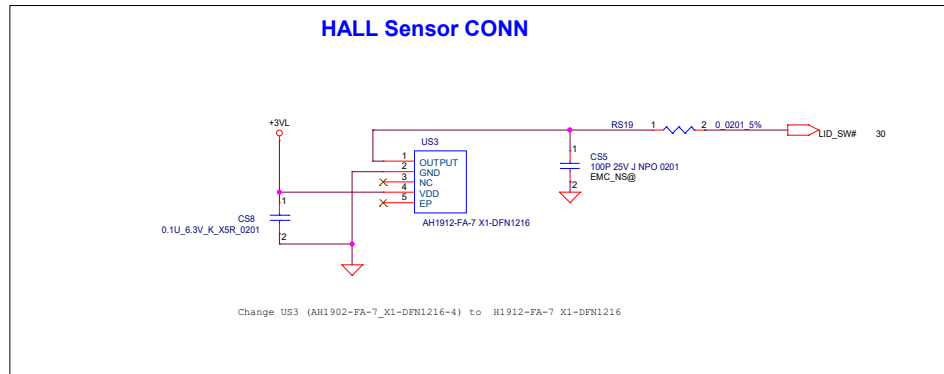
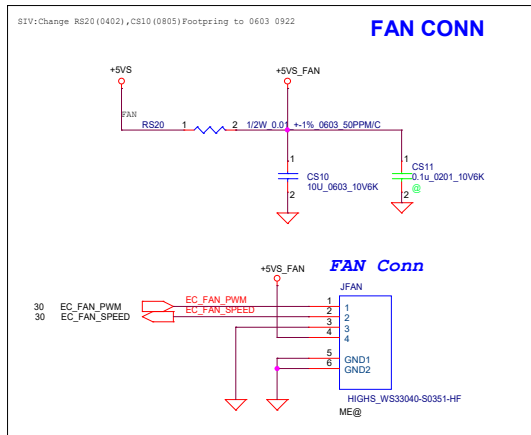
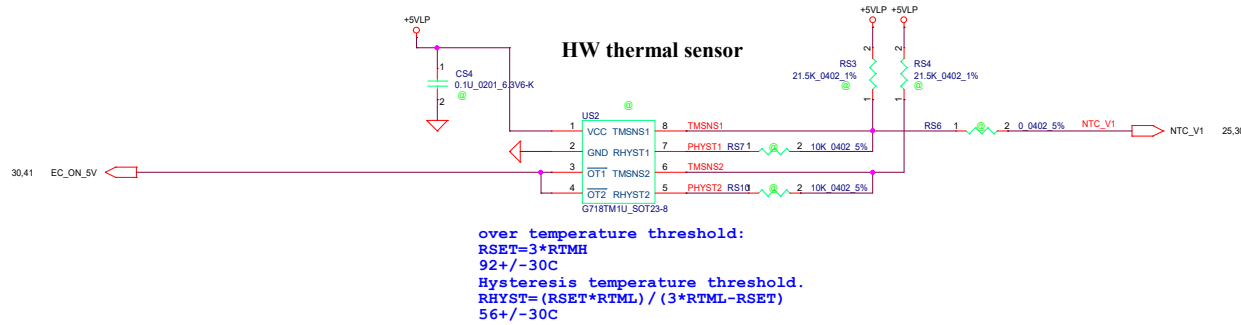
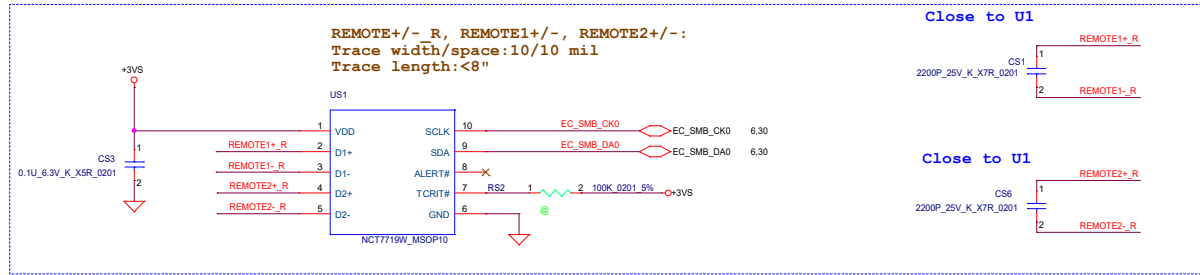
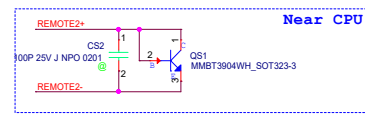
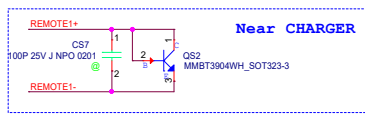
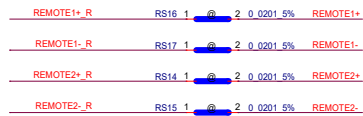
close to JTC PIN A4,A9,B4,B9



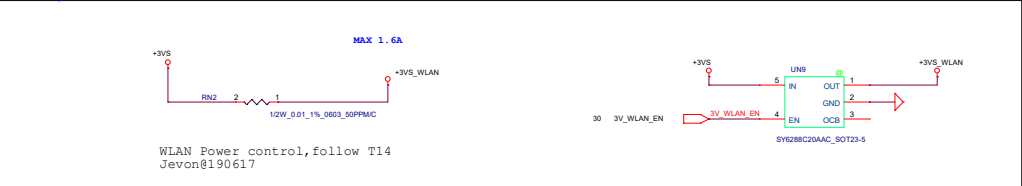
Type C Connector



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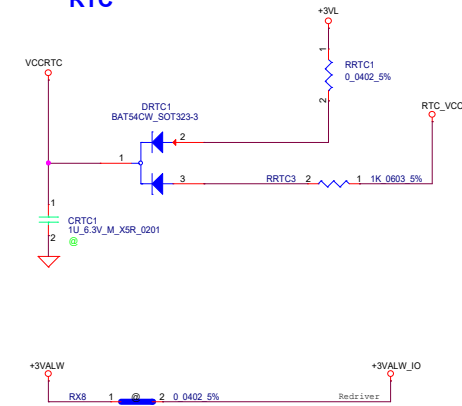
Mini-Express Card(WLAN/WiMAX)



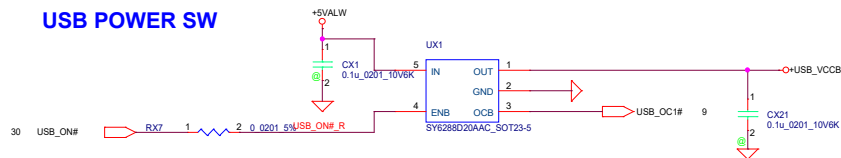
BUTTON



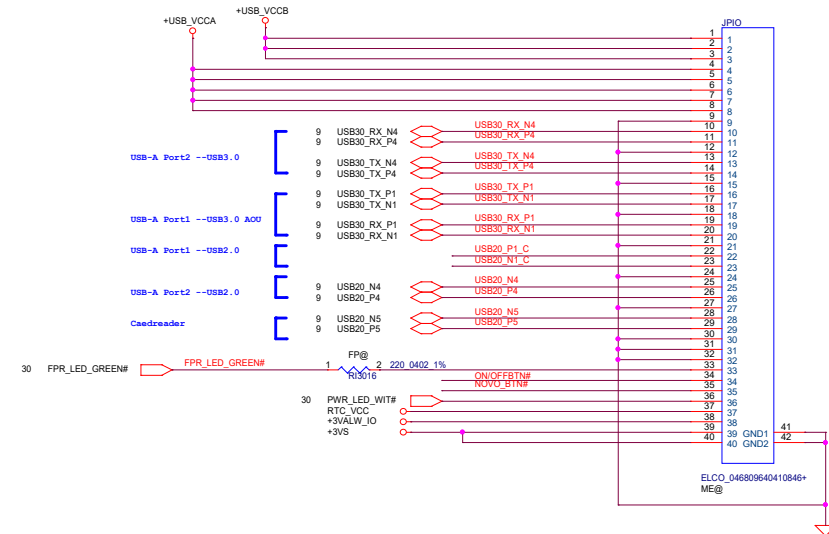
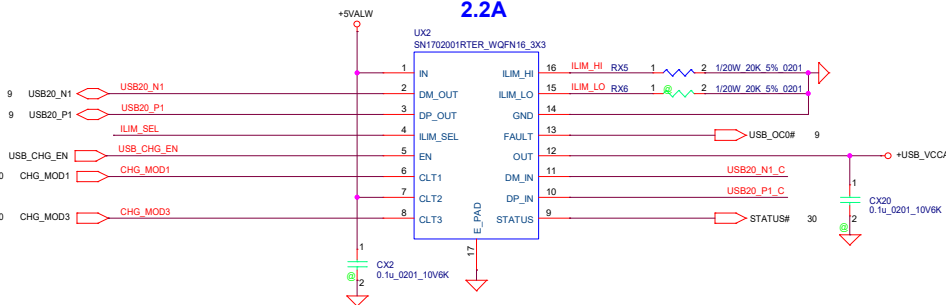
RTC



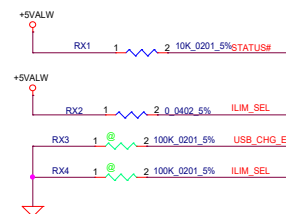
USB POWER SW



USB Charger 2.2A

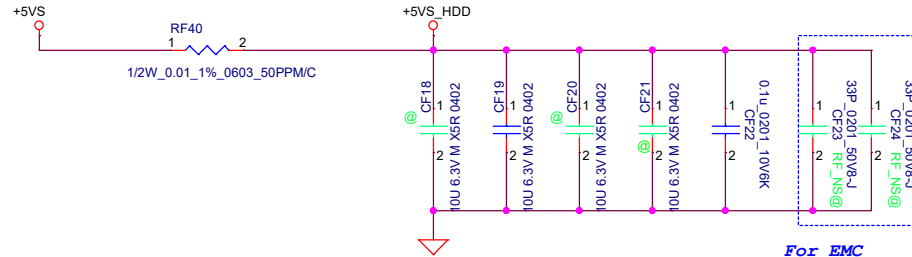


CLT1	CLT2	CLT3	ILIM_SEL	MOD
0	0	0	X	DCH OUT held low
1	1	1	1	CDP Data Connected and Load Detect Active
1	1	1	0	SDP2 Data Connected
1	1	0	X	SDP1 Data Connected
0	1	0	X	SDP1 Data Connected
1	0	0	X	DCP_Short Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto Data Disconnected and Load Detect Active
0	0	1	X	DCP_Auto Data Disconnected and Load Detect Active



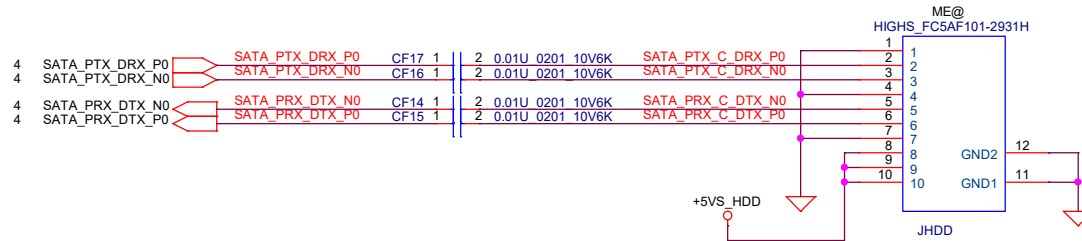
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HDD Power control, MAX 3A
follow S145API 07/26




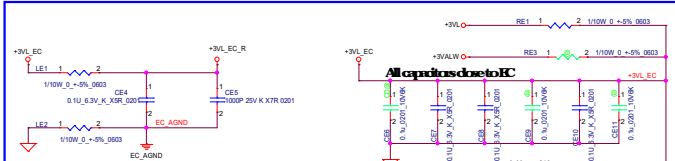
Change CF18-21 to 10U 6.3V/follow S550 Intel for limit hight 0806

SATA HDD Conn.

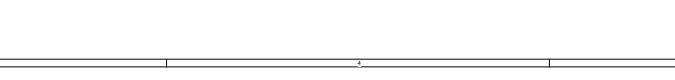
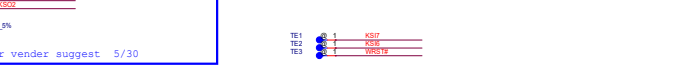
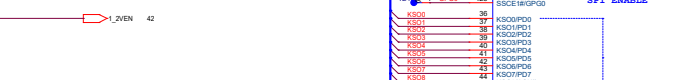
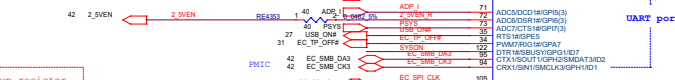
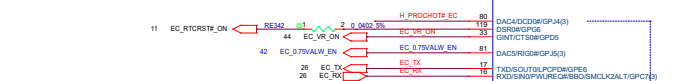
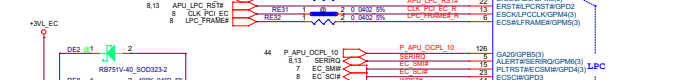
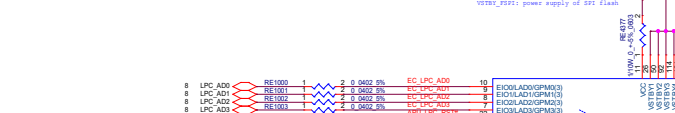


Mirror JHDD For Pin number as same intel S550_1123

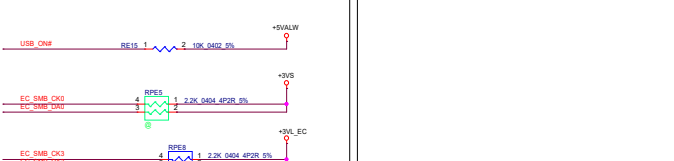
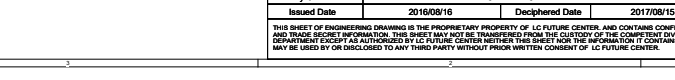
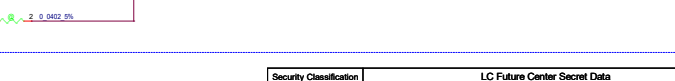
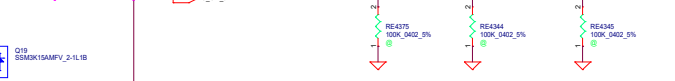
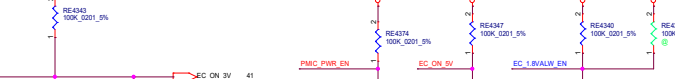
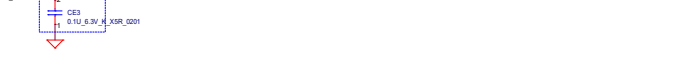
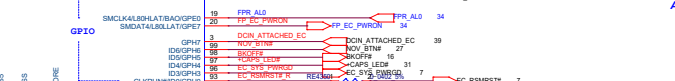
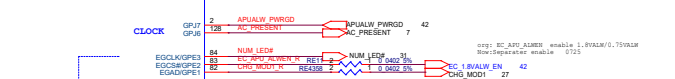
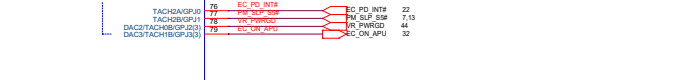
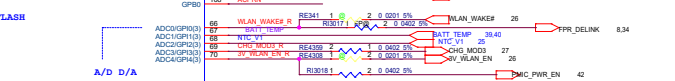
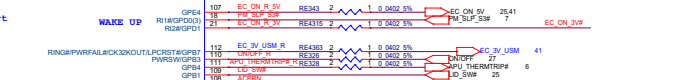
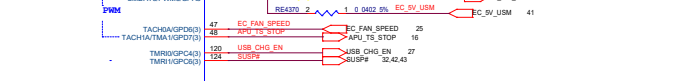
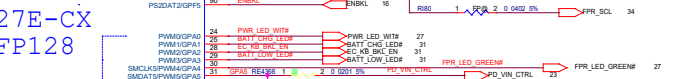
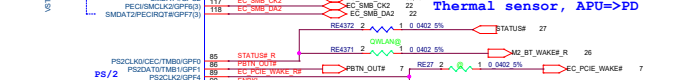
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		Date:		Thursday, November 28, 2019		Sheet 29 of 45	



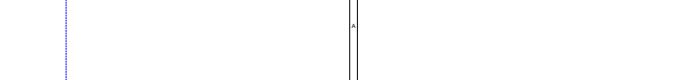
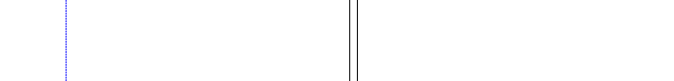
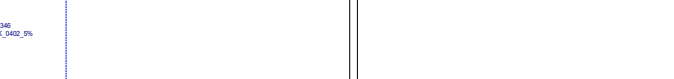
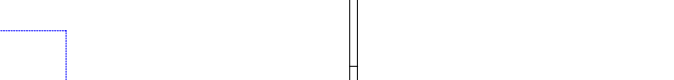
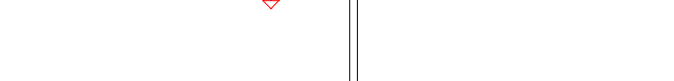
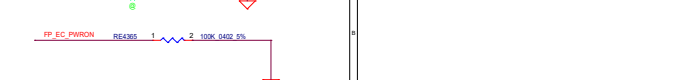
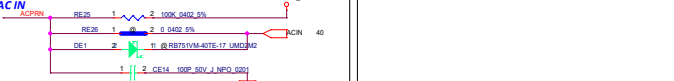
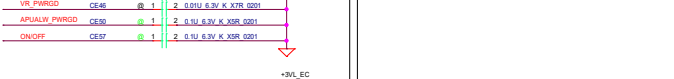
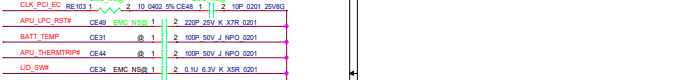
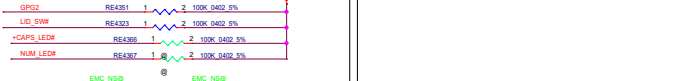
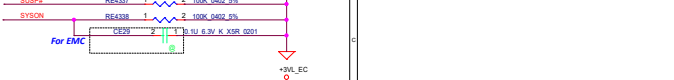
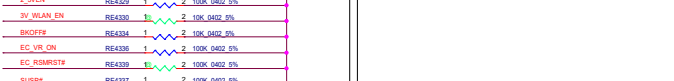
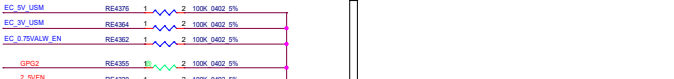
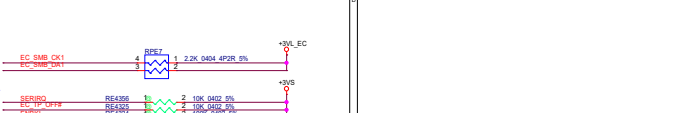
VDD: power supply of LPC
VDDT, PPT1: power supply of PPT flash



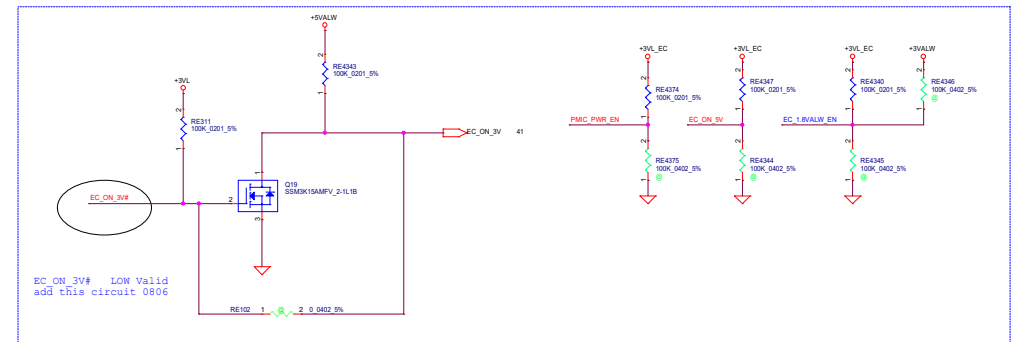
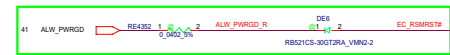
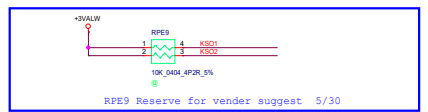
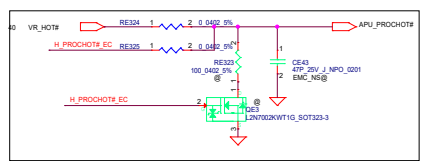
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VDDT, PPT1: power supply of PPT flash



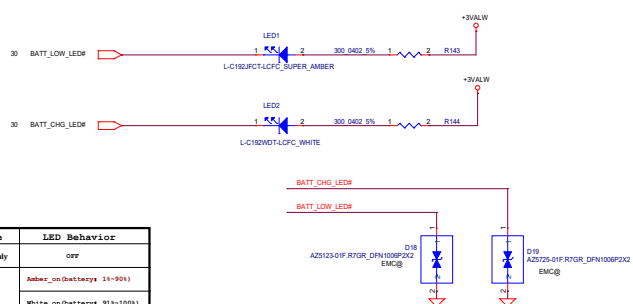
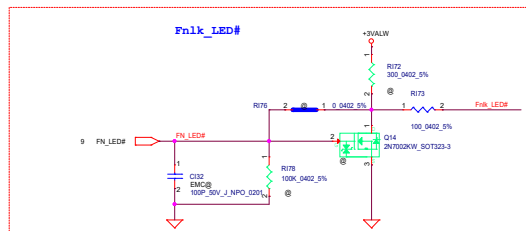
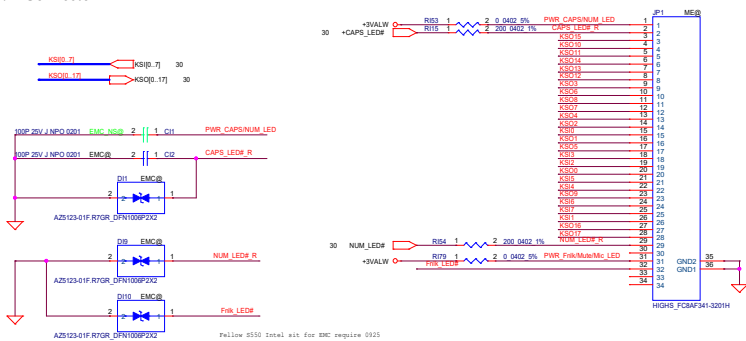
VDD: power supply of LPC
VDDT, PPT1: power supply of PPT flash



Please do not place any pull-up resistor on GP00, GP02, and GP06 (Reserved hardware strapping).



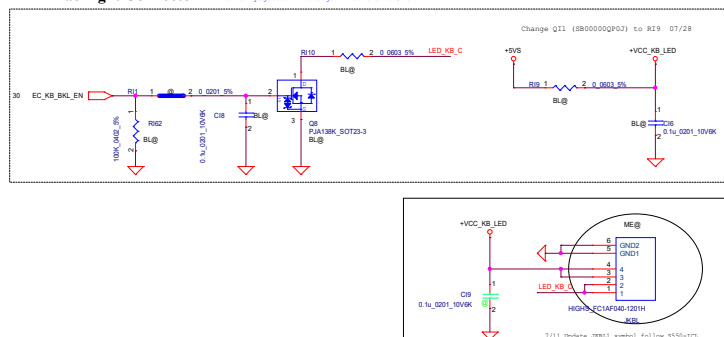
K/B Connector



LED	Stute	LED Behavior
Charge LED	Battery only	OFF
	Charging	Amber_on (Battery: 1%-90%)
		White_on (Battery: 91%-100%)

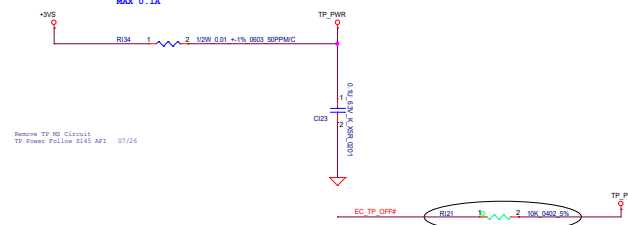
KB Backlight Connector

Follow yogo530-ARR Change BL Control 07/28

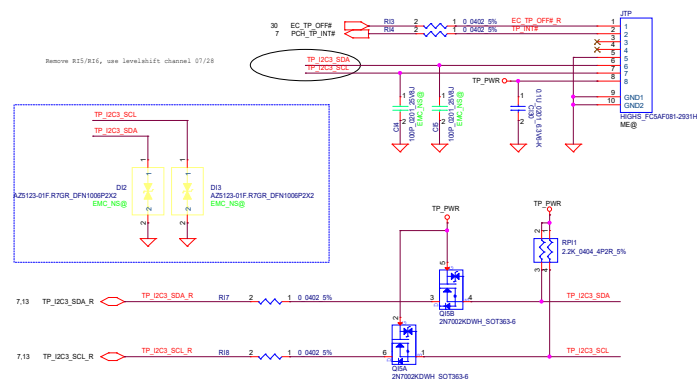


TP Power control,

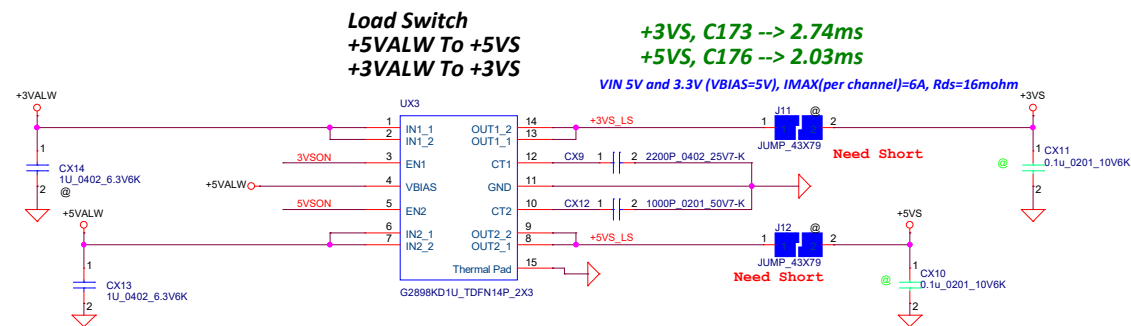
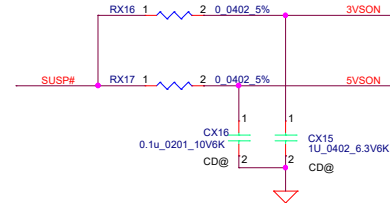
+3VALW TO TP_PWR



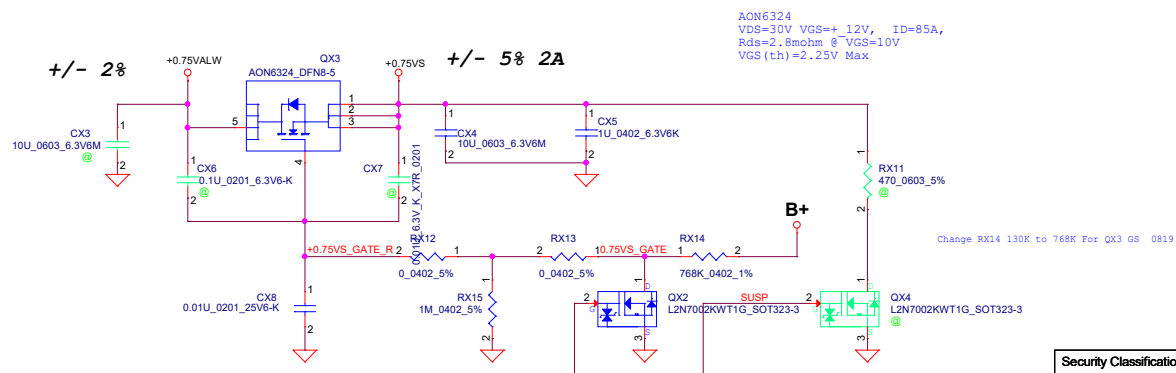
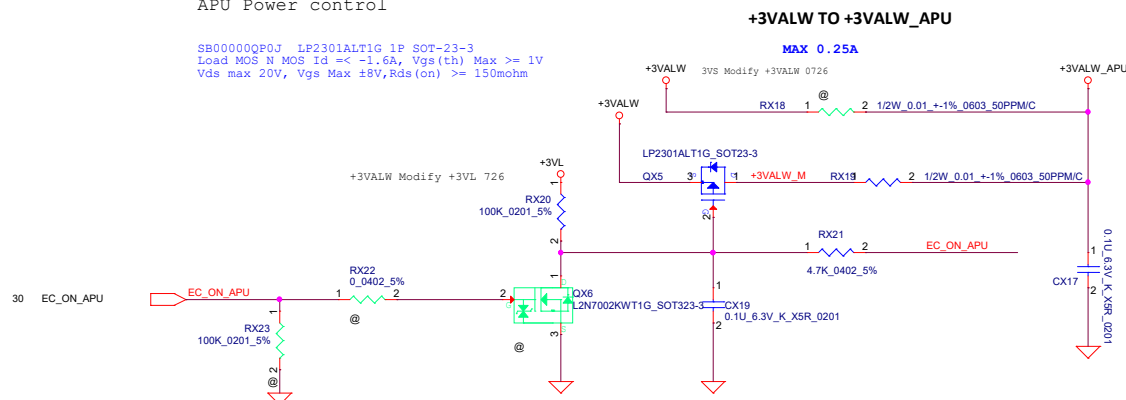
TP/B Connector

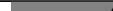


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SB000000QP0J LP2301ALT1G 1P SOT-23-3
Load MOS N MOS Id <= -1.6A, Vgs(th) Max >= 1V
Vds max 20V, Vgs Max ±8V, Rds(on) >= 150mohm

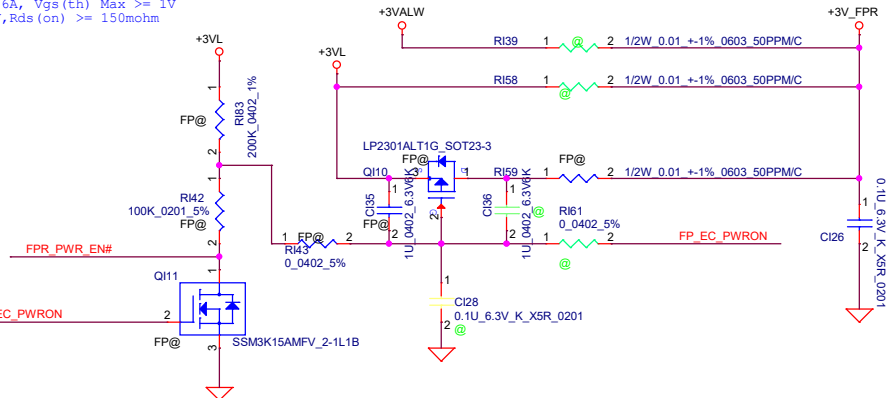


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Date:	Thursday, November 28, 2019	ISheet	32	of 45		

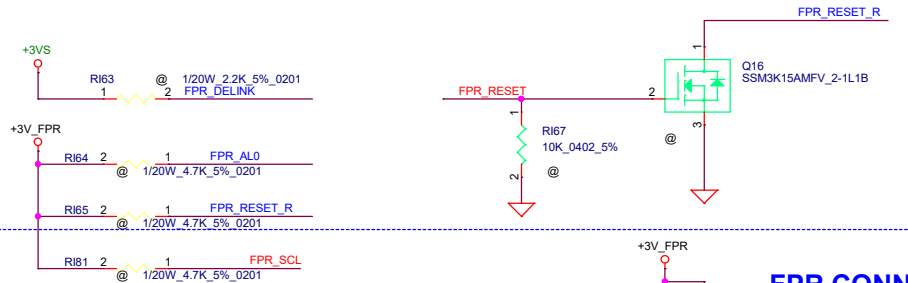
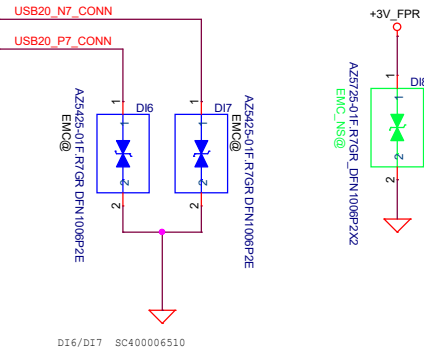
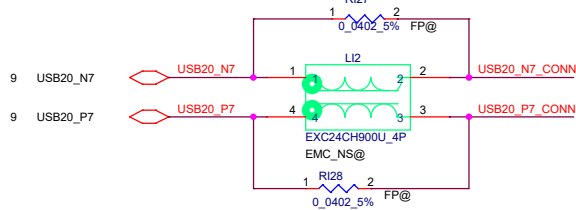
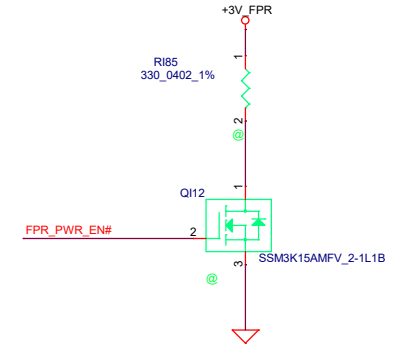
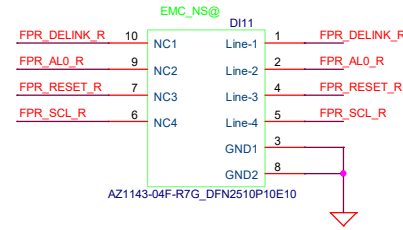


FP Power control, follow T14
 Jevon@190617
 SB00000Q0UJ LP2301ALT1G 1P SOT-23-3
 Load MOS N MOS Id =< -1.6A, Vgs(th) Max >= 1V
 Vds max 20V, Vgs Max ±8V, Rds(on) >= 150mohm

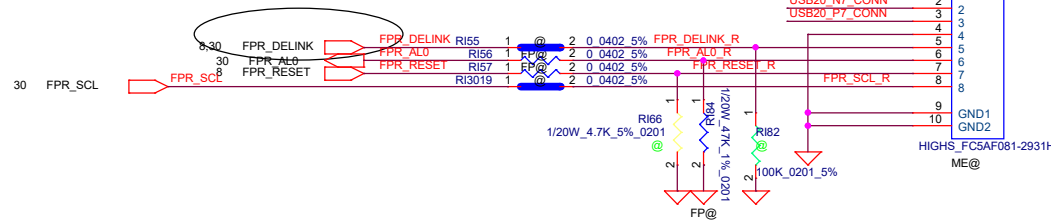
+3VALW TO +3V_FPR







For ESD
 close to Conn



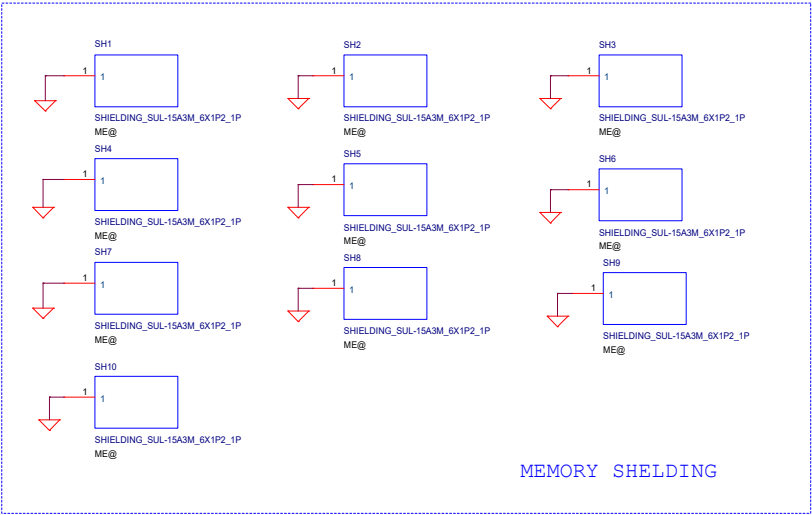
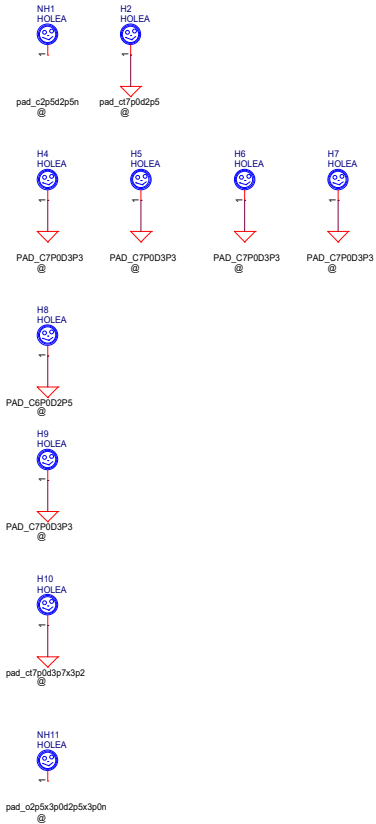
Follow E14 now no connect APU&EC ,Tracking 07/30



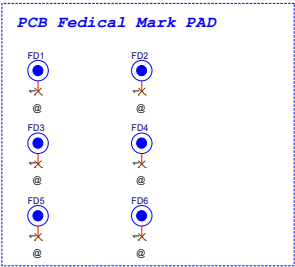
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Date:		Thursday, November 28, 2019		Sheet 34 of 45			

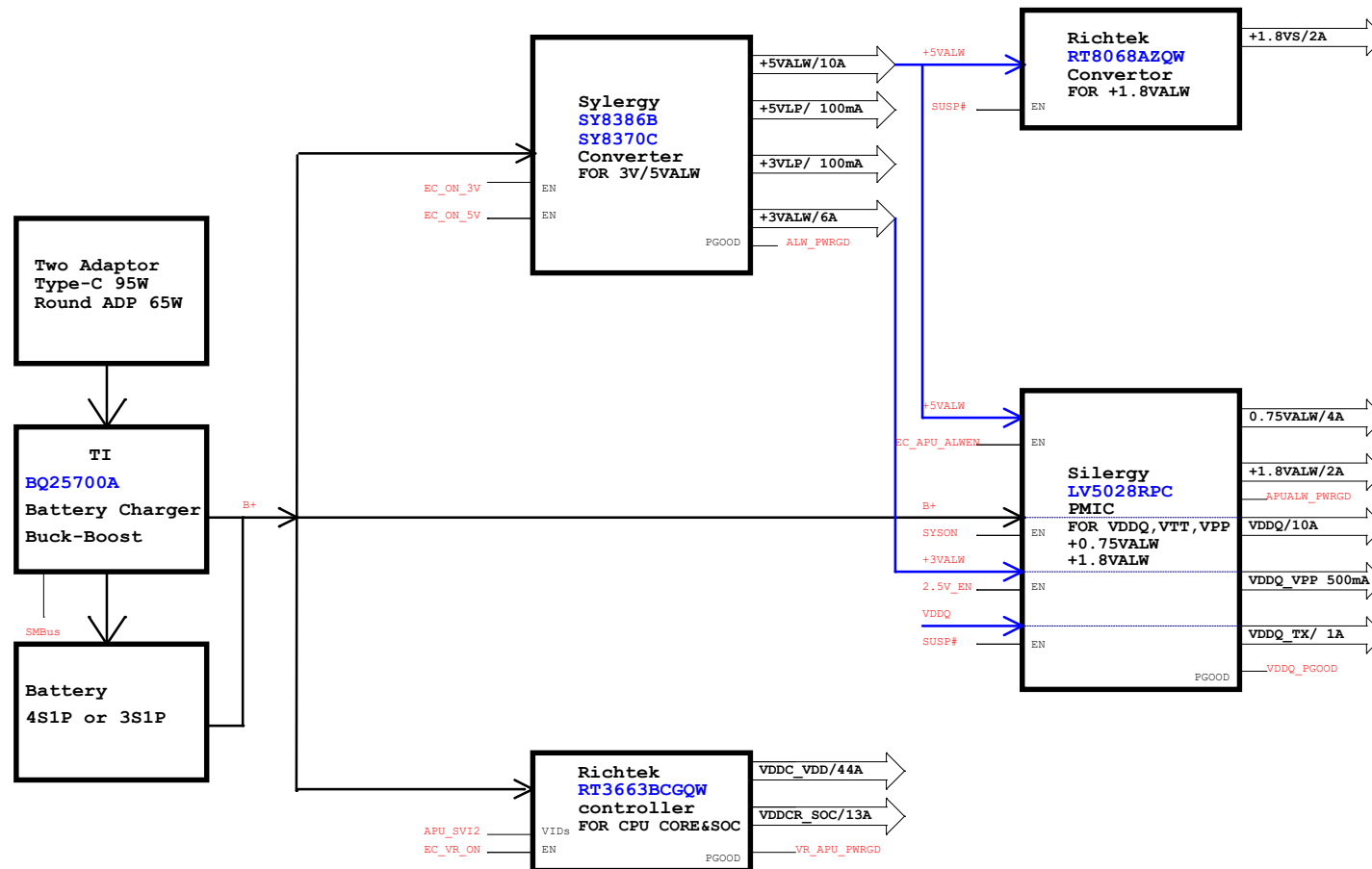
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D				D																														
C				C																														
B				B																														
A				A																														
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Issued Date	2013/08/15	Deciphered Date	2013/08/15	Power sequence Block																														
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Date:	Thursday, November 28, 2019	Sheet	35	of 45																														
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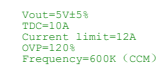
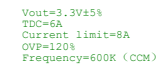
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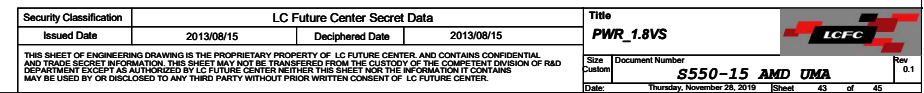


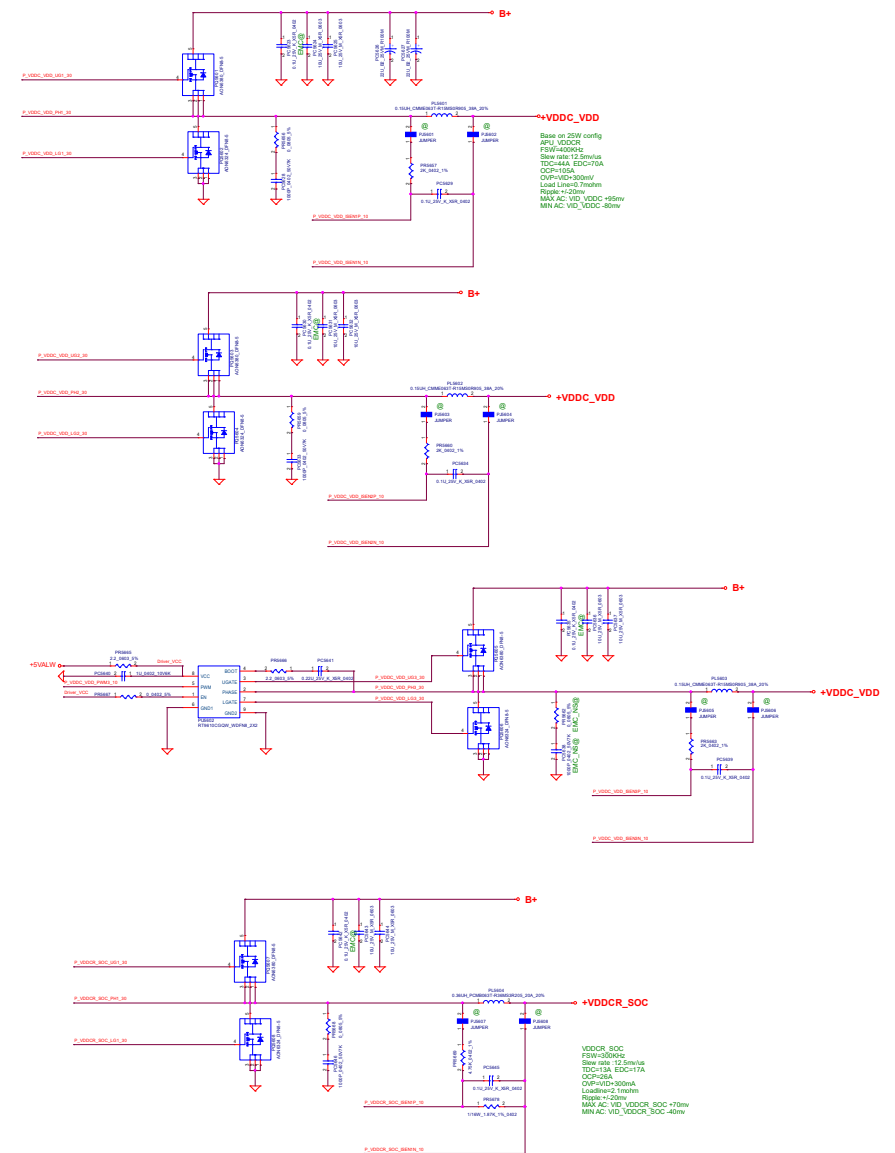
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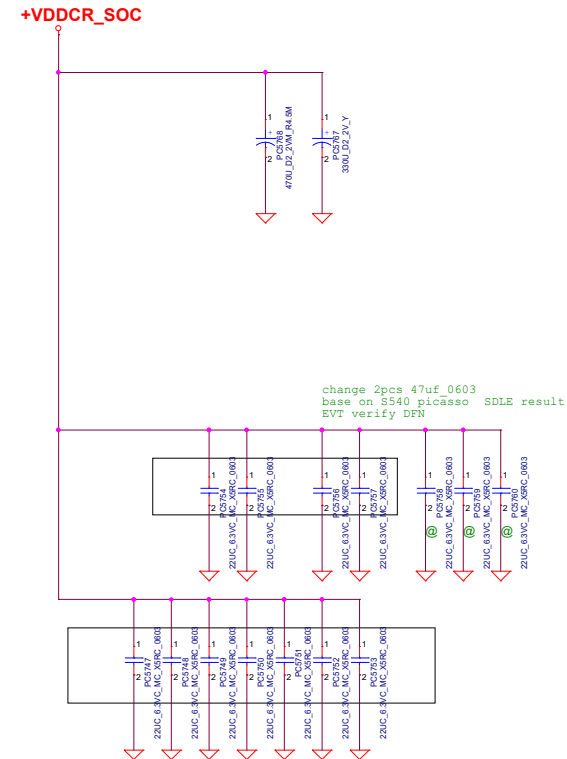
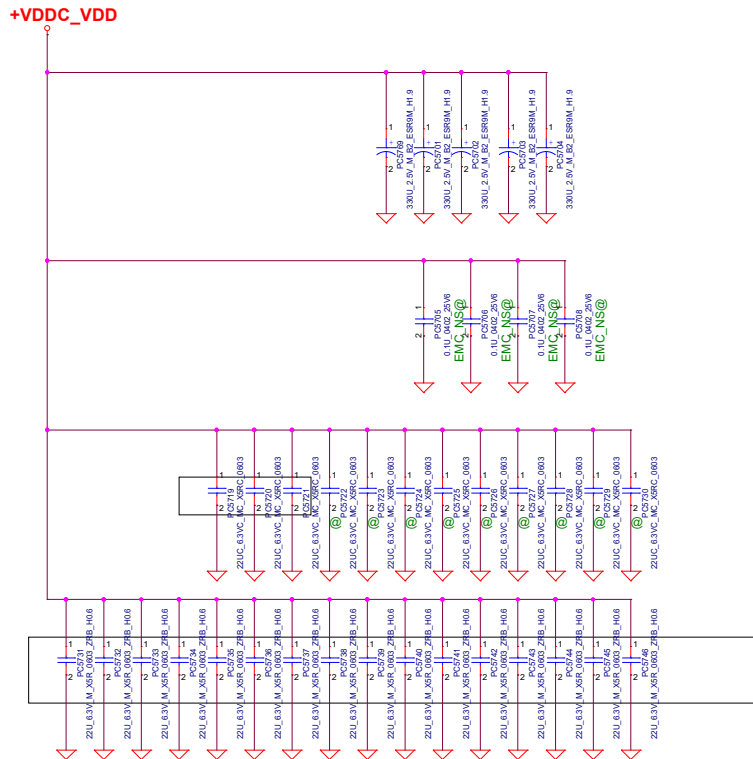












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